SHARC® Melody® Ultra Audio Processor

ADSST-SHARC-Melody-Ultra

SUMMARY

High performance 32-bit audio processor

Super Harvard Architecture Computer (SHARC)

4 independent buses for dual data, instruction, and nonintrusive, zero-overhead I/O fetch on a single cycle

Code compatible with all other SHARC family DSPs

Single-instruction-multiple-data (SIMD) computational architecture—two 32-bit IEEE floating-point computation units, each with a multiplier, ALU, shifter, and register file

Serial ports offer I²S support via 8 programmable and simultaneous receive or transmit pins, which support up to 16 transmit or 16 receive channels of audio

Integrated peripherals—integrated I/O processor, 1 Mbit on-chip dual-ported SRAM, SDRAM controller, glueless multiprocessing features, and I/O ports (serial, link, external bus, SPI®, and JTAG)

SHARC Melody Ultra supports 32-bit fixed-point, 32-bit floating-point, and 40-bit floating-point formats

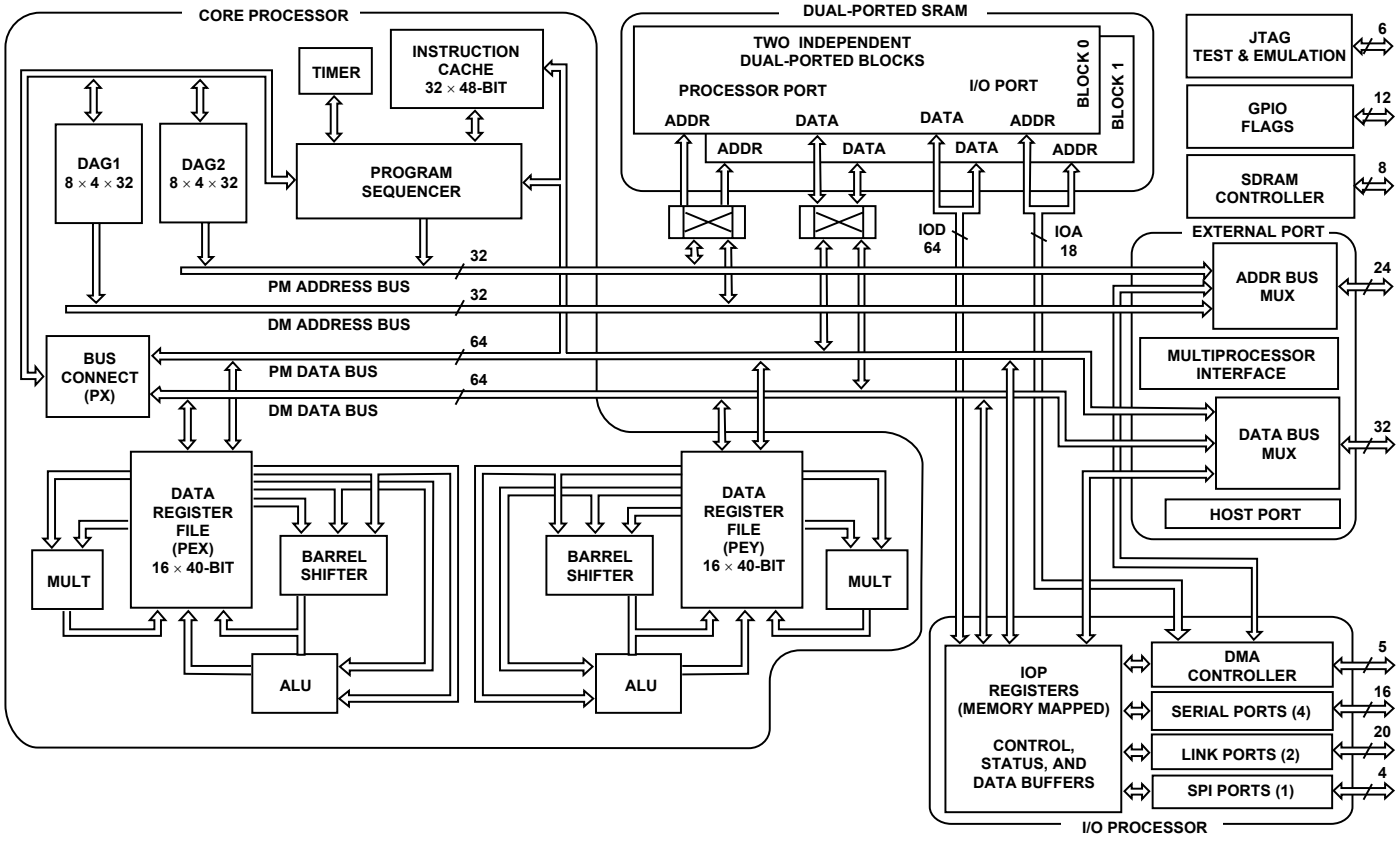

Figure 1. Functional Block Diagram

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

Revision 0: Initial Version

KEY FEATURES

100 MHz (10 ns) core instruction rate

Single-cycle instruction execution, including SIMD operations in both computational units

600 Mflops peak and 400 Mflops sustained performance

225-ball 17 mm × 17 mm MBGA package

Decodes industry-standard formats, using a 32-bit floating-point implementation

Decoders:

- **Dolby® Digital, Dolby Pro Logic® II**
- **Dolby Virtual Speaker Technology, Dolby Headphone™**
- **DTS-ES® Extended Surround (including DTS-ES Discrete and DTS-ES Matrix), DTS-96/24, DTS Neo:6®**
- **THX® Ultra2™**
- **SRS® Labs Circle Surround® II**
- **MPEG2 (MC), MP3 (MPEG1 Audio Layer 3)**
- **PCM**
- **HDCD**
- **Delay Management**
- **Bass Management**
- **MPEG-2 AAC**
- **WaveSurround® virtual loudspeaker, virtual headphone**
- **Downsampling 96 kHz to 48 kHz (2-channel)**

Encoders:

- **Dolby Digital Consumer Encoder**

Single-chip DSP based implementation of digital audio algorithms

SHARC Melody Ultra processor features 100 MIPS and extensive on-chip memory

I^2S compatible serial ports

Interface to external SDRAM

Easy interfaces to audio codecs

192 kHz processing

Supports customer specific postprocessing

Automatic stream detection

Automatic code loading

Easy-to-use software architecture

Optimized library of routines

Host communication using SPI port

Supports IEC 60958 for bit streams

8-channel output

GENERAL DESCRIPTION

The SHARC Melody Ultra family of powerful 32-bit audio processors from Analog Devices enables flexible designs and delivers a host of features across high-end and high fidelity audio systems to the AV receiver and DVD markets. It includes multichannel audio decoders, encoders, and postprocessors for digital audio designs using DSPs in home theater systems and automotive audio receivers.

With 32-bit audio quality, the SHARC Melody Ultra audio processor autodetects and decodes audio formats in real time, enabling end users to enjoy a theater-quality audio experience in their homes and automobiles.

The designs can be customized to meet the exact requirements of the application. This audio DSP system enables designers to make value additions to product features working off the high-end base functionality with which they are provided.

Evaluation boards, sample applications and all necessary software support (e.g., drivers) are available. The evaluation board enables OEMs to offer comprehensive and single-chip implementations of advanced features for end-user products. SHARC Melody Ultra audio processors enable OEMs to produce high quality, low cost designs featuring decoder algorithms and postprocessors for DTS-ES Extended Surround (including both DTS Discrete 6.1 and DTS Matrix 6.1), DTS Neo:6, Dolby Digital, Dolby Pro Logic II, Dolby Headphone, Dolby Virtual Speaker Technology, THX Ultra2, HDCD, MPEG1 Audio Layer 3 (also known as MP 3), MPEG2 multichannel, AAC, WaveSurround, SRS Labs' Circle Surround II, and stereo. It additionally includes audio encoders for DDCE.

The cost of development is reduced, enabling common solutions across product lines. Field and remotely upgradeable products with programmable DSPs and an optimized library of routines, along with the best development tools in the industry, reduce the time to market.

SHARC Melody Ultra is the comprehensive answer to the needs of the high-end, high quality digital audio market. It delivers a realistic high fidelity audio experience along with the maximum number of features in the product, across price points in the high-end home theater and DVD markets.

HARDWARE ARCHITECTURE

Hardware architecture includes the interface between the DSP and the host microcontroller, command processing, data transfer in serial and parallel form, data buffer management, algorithm combinations, MIPS, and memory requirements that are provided.

The multichannel algorithms are implemented on a SHARC Melody Ultra AVR evaluation board. The board is standalone and accepts a compressed digital bit stream as serial input from LD/DVD/CD players or stream generators, decodes the bit stream, and generates a PCM stream in real time in 2-channel or multichannel mode. It has a microcontroller to handle commands and option selections from a small keypad and an LCD display for status display.

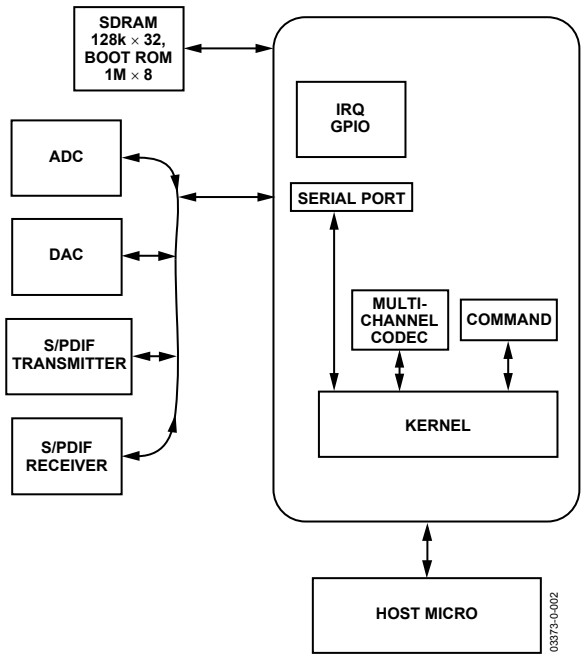

Figure 2. Simplified Block Diagram

To understand the SHARC Melody Ultra family hardware architecture, one should examine its four major blocks:

- The Core Processor
- Dual-Ported SRAM
- External Port
- Input/Output Processor

The hardware architecture of the SHARC Melody Ultra is complex. It has four independent buses for dual data, one for instructions, and one for I/O fetch. Since the four buses are independent, multiple transactions take place within a single clock cycle. It has two external ports, DMA channels, and eight serial ports. It is a 0.35 ns technology IC operating at 3.3 V.

The SHARC Melody Ultra processor can be interfaced to external peripherals with relative ease. The communication between the SHARC Melody Ultra processor and a host microcontroller utilizes the SPI bus. The host microcontroller can be the master and the SHARC Melody Ultra processor can act as a slave. The peripherals can be controlled by the host microcontroller using the SPI bus. The communication is based on commands and parameters. Status information regarding the SHARC Melody Ultra decoding is periodically updated and made available to the host microcontroller.

The block diagram of the SHARC Melody Ultra (see Figure 1) illustrates the following architectural features:

- Computation units (ALU, multiplier, and shifter) with a shared data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- Timers with event capture modes
- On-chip, dual-ported SRAM
- External port for interfacing to off-chip memory and peripherals
- Host port and SDRAM interface
- DMA controller
- Enhanced serial ports
- JTAG test access port

We will use Figure 2 as our reference. The SHARC Melody Ultra communicates with the host microcontroller using SPI. The SHARC Melody Ultra has an on-chip memory buffer that is used for storing commands/parameters sent by the host to the SHARC Melody Ultra and status information from the SHARC Melody Ultra. There is a defined protocol for passing commands and obtaining status information. Once the SHARC Melody Ultra receives a command from the host micro, it will process the command and inform the host micro about the status. These commands initiate actions such as encoding and decoding. Encoding and decoding will result in data processing and the processed data may be delivered over the serial port. For example, while encoding, the MP3 data is accepted through the serial port from peripherals like an ADC or S/PDIF receiver. The MP3 data is then encoded and stored in an on-chip compressed data buffer. The SHARC Melody Ultra will prepare the compressed frames in IEC 958 format so that they can be sent out using the serial port or S/PDIF transmitter. Using the serial port, compressed frames can be downloaded to the SHARC Melody Ultra where they can be decoded, and the resulting MP3 data can be sent on the serial port transmitter. While commands and data are transferred between the host microcontroller and the SHARC Melody Ultra over the SPI, reliable communication needs the help of interrupts and a few general-purpose input/output lines.

SOFTWARE ARCHITECTURE

The audio processors from Analog Devices enable designers to make value additions to product features working off the high-end base functionality. The SHARC Melody Ultra software has the following parts:

- Executive kernel
- Algorithm as library module

The executive kernel has the following functions:

- Power-up hardware initialization
- Serial port management
- Automatic stream detect
- Automatic code load
- Command processing
- Interrupt handling
- Data buffer management
- Calling library module
- Status report

The executive kernel is executed as soon as booting takes place. The hardware resources are initialized in the beginning. The command buffer and general-purpose programmable flag pins are initialized. Various data buffers and memory variables are initialized. Interrupts are programmed and enabled. Then, definite signatures are written "Command buffer" to inform the host that the SHARC Melody Ultra is ready to receive the commands. Once commands are issued by the host microcontroller, they are executed and appropriate actions take place. Decoding is handled by issuing appropriate commands from the host microcontroller.

The kernel communicates with the library module for a particular algorithm in a defined way. The details are found in the specific implementation documents. As the kernel is modular, it is easy to customize to different hardware platforms. Most of the time, users need to change the initialization code to suit the particular codec chosen.

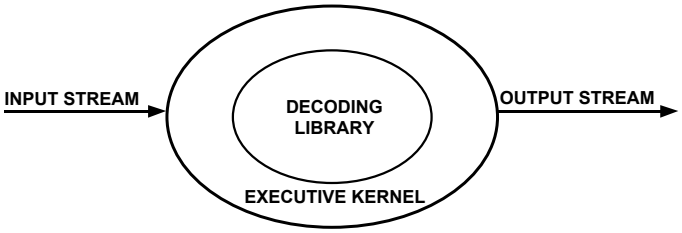

Figure 3. Software

The SHARC Melody Ultra includes a 100 MHz core, dual-ported on-chip SRAM, an integrated I/O processor with multiprocessing support, and multiple internal buses to eliminate I/O bottlenecks. The SHARC Melody Ultra offers a Single-Instruction-Multiple-Data (SIMD) architecture, using two computational units. Fabricated in a state of the art, high speed, low power CMOS process, the SHARC Melody Ultra has a 10 ns instruction cycle time.

With its SIMD computational hardware running at 100 MHz, the SHARC Melody Ultra can perform 600 million math operations per second. Table 1 shows performance benchmarks for the SHARC Melody Ultra.

The SHARC Melody Ultra continues the SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include a 1 Mbit dual-ported SRAM memory, a host processor interface, an I/O processor that supports 14 DMA channels, four serial ports, two link ports, an SDRAM controller, an SPI interface, an external parallel bus, and glueless multiprocessing.

Figure 2 illustrates the following architectural features:

- Two processing elements, each made up of an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core every core processor cycle
- Interval timer
- On-chip SRAM (1 Mbit)
- SDRAM controller for glueless interface to SDRAMs
- External port that supports
  - Interfacing to off-chip memory peripherals
  - Glueless multiprocessing for six SHARC Melody Ultra processors
  - Host port read/write of IOP registers
- DMA controller
- Four serial ports
- Two link ports
- SPI compatible interface
- JTAG test access port
- 12 general-purpose I/O pins

Figure 4 shows a typical single-processor system. A multiprocessing system appears in Figure 7.

SHARC MELODY ULTRA FAMILY CORE ARCHITECTURE

The SHARC Melody Ultra includes the following architectural features of the ADSP-2116x family core:

SIMD Computational Engine

The SHARC Melody Ultra contains two computational processing elements that operate as a Single Instruction Multiple Data (SIMD) engine. The processing elements are referred to as PEX and PEY, and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math-intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform single-cycle instructions. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Table 1. Benchmarks (at 100 MHz)

Benchmark Algorithm	Speed (at 100 MHz)
1024 Point Complex FFT (Radix 4, with Reversal)[1]	171 µs
FIR Filter (per Tap)[1]	5 ns
IIR Filter (per Biquad)[1]	40 ns
Matrix Multiply (Pipelined)	
[3 × 3] • [3 × 1]	30 ns
[4 × 4] • [4 × 1]	37 ns
Divide (y/x)	60 ns
Inverse Square Root	40 ns
DMA Transfers	800 Mbytes/s

[1]Assumes two filters in multichannel SIMD mode

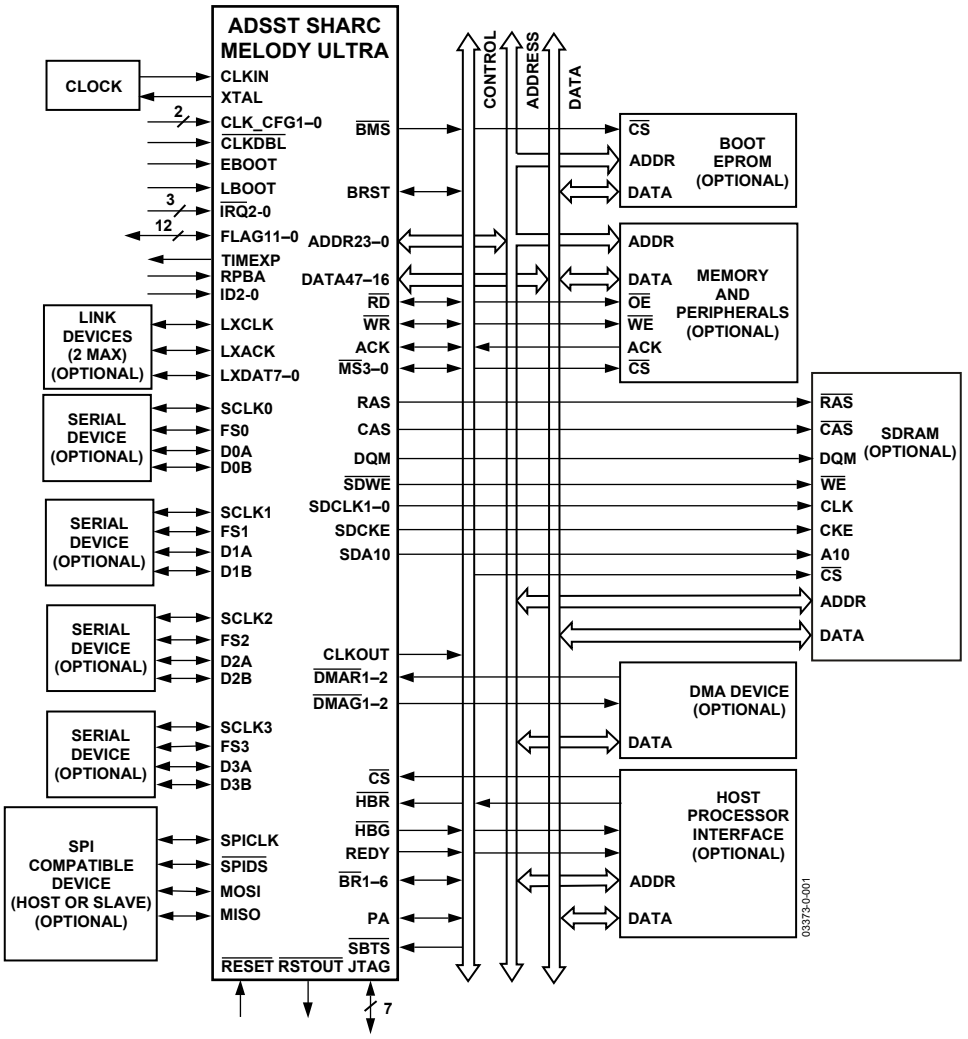

Figure 4. System Block Diagram

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the SHARC Melody Ultra's enhanced Harvard architecture, enable unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15, and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The SHARC Melody Ultra features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 4). With the SHARC Melody Ultra's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and an instruction (from the cache), all within a single cycle.

Instruction Cache

The SHARC Melody Ultra includes an on-chip instruction cache that enables 3-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache enables full speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The SHARC Melody Ultra processor's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers enable efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the SHARC Melody Ultra contain sufficient registers to enable the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer

wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the SHARC Melody Ultra can conditionally execute a multiply, an add, and a subtract in both processing elements, while branching, all within a single instruction.

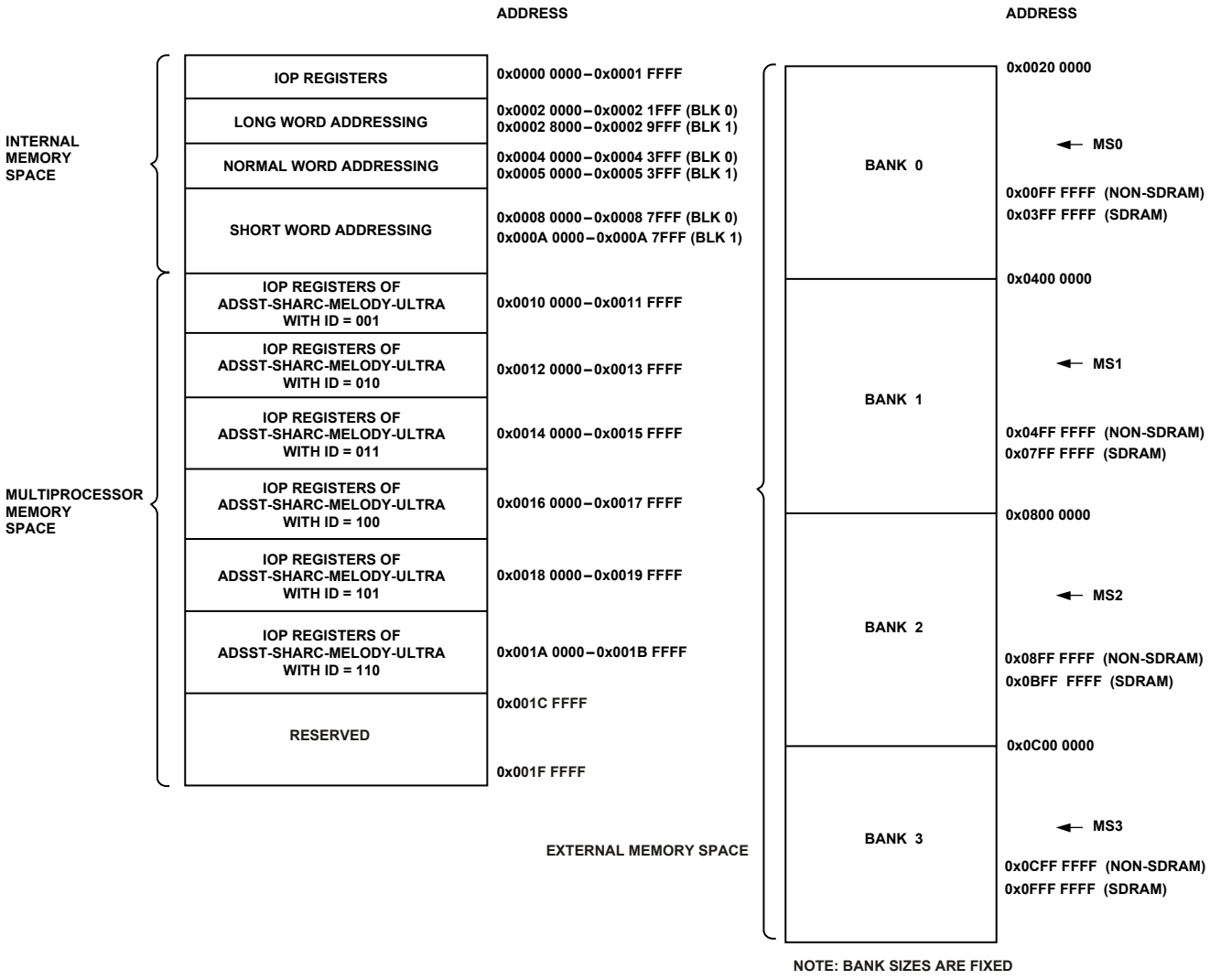

Figure 5. Memory Map Block Diagram

SHARC MELODY ULTRA MEMORY AND I/O INTERFACE FEATURES

The SHARC Melody Ultra adds the following architectural features to the ADSP-2116x family core:

Dual-Ported On-Chip Memory

The SHARC Melody Ultra contains 1 Mbit of on-chip SRAM, organized as two blocks of 0.5 Mbits. Each block can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory in combination with three separate on-chip buses enables two data transfers from the core and one from the I/O processor, within a single cycle. On the SHARC Melody Ultra, the memory can be configured as a maximum of 32 Kwords of 32-bit data, 64 Kwords of 16-bit data, 21 Kwords of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 1 Mbit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. While each memory block can store combinations of code and data, access is most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers. Using the DM bus and PM bus, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

Off-Chip Memory and Peripherals Interface

The SHARC Melody Ultra's external port provides the processor's interface to off-chip memory and peripherals. The 62.7 Mword off-chip address space (254 Mword if all SDRAM) is included in the SHARC Melody Ultra processor's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 24-bit address bus and a single 32-bit data bus. Every access to external memory is based on an address that fetches a 32-bit word. When fetching an instruction from external memory, two 32-bit data locations are being accessed for packed instructions. Unused link port lines can also be used as additional data lines DATA[0]–DATA[15], enabling single-cycle execution of instructions from external memory at up to 100 MHz. Figure 6 shows the alignment of various accesses to external memory.

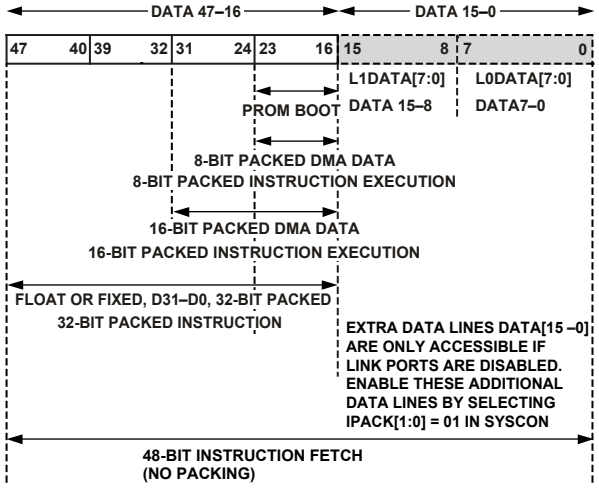

Figure 6. External Data Alignment Options

The external port supports asynchronous, synchronous, and synchronous burst access. Synchronous burst SRAM can be interfaced gluelessly. The SHARC Melody Ultra can also interface gluelessly to SDRAM. Addressing of an external memory device is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. The SHARC Melody Ultra provides programmable memory wait states and external memory acknowledge controls to enable interfacing to memory and peripherals with variable access, hold, and disable time requirements.

SDRAM Interface

The SDRAM interface enables the SHARC Melody Ultra to transfer data to and from synchronous DRAM (SDRAM) at the core clock frequency or one-half the core clock frequency. The synchronous approach, coupled with the core clock frequency, supports data transfer at a high throughput—up to 400 Mbytes/s for 32-bit transfers and 600 Mbytes/s for 48-bit transfers. The SDRAM interface provides a glueless interface with standard SDRAMs (16 Mbit, 64 Mbit, 128 Mbit, and 256 Mbit) and includes options to support additional buffers between the SHARC Melody Ultra and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the SHARC Melody Ultra processor's four external memory banks, with up to all four banks mapped to SDRAM. Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The SHARC Melody Ultra supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Target Board JTAG Emulator Connector

Analog Devices' DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the SHARC Melody Ultra processor to monitor and control the target board processor during emulation. Analog Devices' DSP Tools product line of JTAG emulators provides emulation at full processor speed, enabling inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing. For complete information on Analog Devices' DSP Tools product line of JTAG emulator operation, see the appropriate *Emulator Hardware User's Guide*. For detailed information on the interfacing of Analog Devices' JTAG emulators with Analog Devices' DSP products with JTAG emulation ports, please refer to the Engineer-to-Engineer Note EE-68, *Analog Devices JTAG Emulation Technical Reference*. Both of these documents can be found on the Analog Devices website at: http://www.analog.com/dsp/tech_docs.html.

DMA Controller

The SHARC Melody Ultra processor's on-chip DMA controller enables zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, enabling DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the SHARC Melody Ultra processor's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the SHARC Melody Ultra processor's internal memory and its serial ports, link ports, or the SPI (serial peripheral interface) compatible port. External bus packing and unpacking of 16-, 32-, 48-, or 64-bit words in internal memory is performed during DMA transfers from either 8-, 16-, or 32-bit wide external memory. Fourteen channels of DMA are available on the SHARC Melody Ultra; two are shared between the SPI interface and the link ports, eight via the serial ports, and four via the processor's external port (for either host processor, other SHARC Melody Ultra's memory or I/O transfers). Programs can be downloaded to the SHARC Melody Ultra using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA request/grant lines ($\overline{\text{DMAR}}$1–2, $\overline{\text{DMAG}}$1–2). Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Multiprocessing

The SHARC Melody Ultra offers powerful features tailored to multiprocessing DSP systems. The external port and link ports provide integrated glueless multiprocessing support. The external port supports a unified address space (see Figure 5) that enables direct interprocessor accesses of each SHARC Melody Ultra processor's internal memory-mapped (I/O processor) registers. All other internal memory can be indirectly accessed via DMA transfers initiated through the programming of the IOP DMA parameter and control registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six SHARC Melody Ultra processors and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock enables indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. The maximum throughput for interprocessor data transfers is 400 Mbytes/s over the external port. Two link ports provide a second method of multiprocessing communications. Each link port can support communications to another SHARC Melody Ultra. The SHARC Melody Ultra running at 100 MHz has a maximum throughput for interprocessor communications over the links of 200 Mbytes/s. The link ports and cluster multiprocessing can be used concurrently or independently.

Link Ports

The SHARC Melody Ultra features two 8-bit link ports that provide additional I/O capabilities. With the capability of running at 100 MHz, each link port can support 100 Mbytes/s. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems. The link ports can operate independently and simultaneously, with a maximum data throughput of 200 Mbytes/s. Link port data is packed into 48- or 32-bit words and can be directly read by the core processor, or DMA-transferred to on-chip memory. Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

Serial Ports

The SHARC Melody Ultra features four synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. Each serial port is made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive.

The serial ports operate at up to half the clock rate of the core, providing each with a maximum data rate of 50 Mbps. The serial data pins are programmable as either a transmitter or receiver, providing greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports features a Time Division Multiplex (TDM) multichannel mode; two serial ports are TDM transmitters and two serial ports are TDM receivers (SPORT0 RX paired with SPORT2 TX, SPORT1 RX paired with SPORT3 TX). Each of the serial ports also supports the I^2S protocol (an industry-standard interface commonly used by audio codecs, ADCs, and DACs), with two data pins, enabling four I^2S channels (using two I^2S stereo devices) per serial port, up to a maximum of 16 I^2S channels.

The serial ports enable little-endian or big-endian transmission formats and word lengths selectable from three bits to 32 bits. For I^2S mode, data-word lengths are selectable between eight

bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

Serial Peripheral (Compatible) Interface

Serial Peripheral Interface (SPI) is an industry-standard synchronous serial link, enabling the SHARC Melody Ultra SPI compatible port to communicate with other SPI compatible devices. SPI is a 4-wire interface consisting of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI compatible devices, acting as either a master or slave device. The SHARC Melody Ultra SPI compatible peripheral implementation also features programmable baud rate and clock phase/polarities. The SHARC Melody Ultra SPI compatible port uses open-drain drivers to support a multimaster configuration and to avoid data contention.

Host Processor Interface

The SHARC Melody Ultra host interface enables easy connection to standard 8-bit, 16-bit, or 32-bit microprocessor buses with little additional hardware required. The host interface is accessed through the SHARC Melody Ultra's external port. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead. The host processor requests the SHARC Melody Ultra's external bus with the host bus request ($\overline{HBR}$), host bus grant ($\overline{HBG}$), and ready (REDY) signals. The host can directly read and write the internal IOP registers of the SHARC Melody Ultra, and can access the DMA channel setup and message registers. DMA setup via a host would enable it to access any internal memory address via DMA transfers. Vector interrupt support provides efficient execution of host commands.

General-Purpose I/O Ports

The SHARC Melody Ultra also contains 12 programmable, general-purpose I/O pins that can function as either inputs or outputs. As outputs, these pins can signal peripheral devices; as inputs, these pins can provide the test for conditional branching.

Program Booting

The internal memory of the SHARC Melody Ultra can be booted at system power-up from either an 8-bit EPROM, a host processor, the SPI interface, or through one of the link ports. Selection of the boot source is controlled by the Boot Memory Select ($\overline{BMS}$), EBOOT (EPROM Boot), and Link/Host Boot (LBOOT) pins. 8-, 16-, or 32-bit host processors can also be used for booting.

Phased-Locked Loop and Crystal Double Enable

The SHARC Melody Ultra uses an on-chip phase-locked loop (PLL) to generate the internal clock for the core. The CLK_CFG[1:0] pins are used to select ratios of 2:1, 3:1, and 4:1. In addition to the PLL ratios, the $\overline{CLKDBL}$ pin can be used for more clock ratio options. The (1×/2× CLKIN) rate set by the $\overline{CLKDBL}$ pin determines the rate of the PLL input clock and the rate at which the synchronous external port operates. With the combination of CLK_CFG[1:0] and $\overline{CLKDBL}$, ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 between the core and CLKIN are supported. See Figure 13.

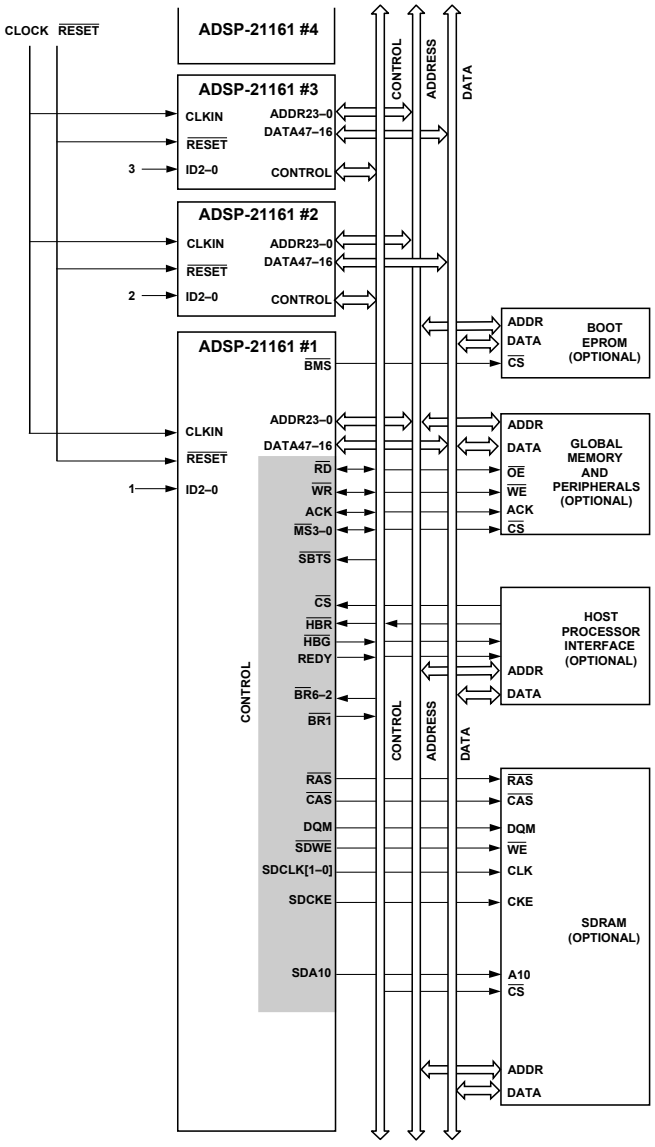

Figure 7. Shared Memory Multiprocessing System

Power Supplies

The SHARC Melody Ultra has separate power supply connections for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (AV_{DD}/AGND) power supplies. The internal and analog supplies must meet the 1.8 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same supply.

Note that the analog supply (AV_{DD}) powers the SHARC Melody Ultra processor's clock generator PLL. To produce a stable clock, provide an external circuit to filter the power input to the AV_{DD} pin. Place the filter as close as possible to the pin. For an example circuit, see Figure 8. To prevent noise coupling, use a wide trace for the analog ground (AGND) signal and install a decoupling capacitor as close as possible to the pin.

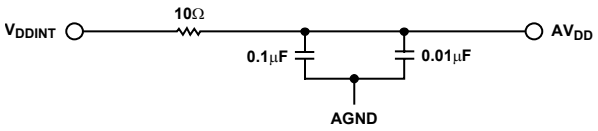

Figure 8. Analog Power (AV_{DD}) Filter Circuit

PIN FUNCTION DESCRIPTIONS

The SHARC Melody Ultra pin definitions can be found in Table 2 beginning on page 14. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

- ADDR23–0, DATA47–0, BRST, CLKOUT. (Note that these pins have a logic level hold circuit enabled on the SHARC Melody Ultra DSP with ID2–0 = 00x.)
- $\overline{\text{PA}}$, ACK, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{DMARx}}$, $\overline{\text{DMAGx}}$, (ID2–0 = 00x). (Note that these pins have a pull-up enabled on the SHARC Melody Ultra DSP with ID2–0 = 00x.)
- LxCLK, LxACK, LxDAT7–0 (LxPDRDE = 0). (See the Link Port Buffer Control Register Bit definitions in the *SHARC Melody Ultra DSP Hardware Reference*.)
- DxA, DxB, SCLKx, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS,$\overline{\text{TRST}}$, TDI. (Note that these pins have a pull-up.)

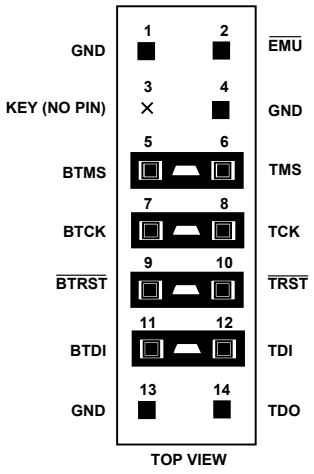

Figure 9. JTAG Target Board Connector for JTAG Equipped Analog Devices DSP (Jumpers in Place)

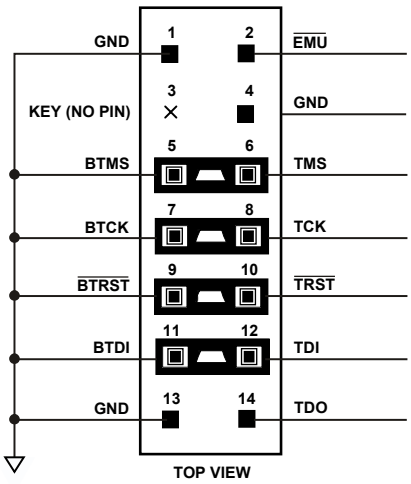

Figure 10. JTAG Target Board Connector with No Local Boundary Scan

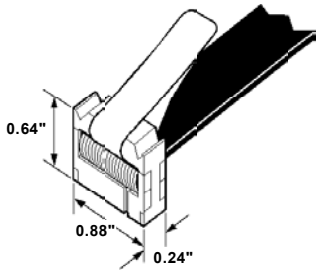

Figure 11. JTAG Pod Connector Dimensions

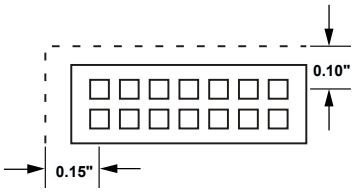

Figure 12. JTAG Pod Connector Keep-Out Area

The following symbols appear in the Type column of Table 2:

A	Asynchronous,
G	Ground,
I	Input,
O	Output,
P	Power Supply,
S	Synchronous,
(A/D)	Active Drive,
(O/D)	Open Drain,
T	Three-State (when $\overline{\text{SBTS}}$ is asserted or when the SHARC Melody Ultra is a bus slave).

Unlike previous SHARC processors, the SHARC Melody Ultra contains internal series resistance equivalent to 50 Ω on all input/output drivers except the CLKIN and XTAL pins. Therefore, for traces longer than six inches, external series resistors on control, data, clock, or frame sync pins are not required to dampen reflections from transmission line effects for point-to-point connections. However, for more complex networks such as star configurations, series termination is still recommended.

Table 2. Pin Function Description

Mnemonic	Type	Function
ACK	I/O/S	**Memory Acknowledge**. External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The SHARC Melody Ultra deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. ACK has a 20 kΩ internal pull-up resistor that is enabled during reset or on DSPs with ID2–0 = 00x.
ADDR23–0	I/O/T	**External Bus Address**. The SHARC Melody Ultra outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes of the IOP registers of other SHARC Melody Ultra processors, while all other internal memory resources can be accessed indirectly via DMA control (that is, accessing IOP DMA parameter registers). The SHARC Melody Ultra inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers. A keeper latch on the DSP's ADDR23–0 pins maintains the input at the level to which it was last driven. This latch is only enabled on the SHARC Melody Ultra with ID2–0 = 00x.
AGND	G	**Analog Power Supply Return.**
AV_{DD}	P	**Analog Power Supply**. Nominally +1.8 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. See the Power Supplies section.
$\overline{\text{BMS}}$	I/O/T	**Boot Memory Select**. Serves as an output or input as selected with the EBOOT and LBOOT pins; see Table 3 on page 18. This input is a system configuration selection that should be hardwired. For Host and EPROM boot, DMA Channel 10 (EPB0) is used. For Link boot and SPI boot, DMA Channel 8 is used. Three-state only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).
BMSTR	O	**Bus Master Output**. In a multiprocessor system, indicates whether the SHARC Melody Ultra is current bus master of the shared external bus. The SHARC Melody Ultra drives BMSTR high only while it is the bus master. In a single-processor system (ID = 000), the processor drives this pin high.
$\overline{\text{BR}}$6–1	I/O/S	**Multiprocessing Bus Requests**. Used by multiprocessing SHARC Melody Ultra processors to arbitrate for bus mastership. A SHARC Melody Ultra only drives its own $\overline{\text{BR}}$x line (corresponding to the value of its ID2–0 inputs) and monitors all others. In a multiprocessor system with less than six SHARC Melody Ultra processors, the unused $\overline{\text{BR}}$x pins should be pulled high; the processor's own $\overline{\text{BR}}$x line must not be pulled high or low because it is an output.
BRST	I/O/T	**Sequential Burst Access**. BRST is asserted by SHARC Melody Ultra to indicate that data associated with consecutive addresses is being read or written. A slave device samples the initial address and increments an internal address counter after each transfer. The incremented address is not pipelined on the bus. A master SHARC Melody Ultra in a multiprocessor environment can read slave external port buffers (EPBx) using the burst protocol. BRST is asserted after the initial access of a burst transfer. It is asserted for every cycle after that, except for the last data request cycle (denoted by $\overline{\text{RD}}$ or $\overline{\text{WR}}$ asserted and BRST negated). A keeper latch on the DSP's BRST pin maintains the input at the level to which it was last driven. This latch is only enabled on the SHARC Melody Ultra with ID2–0 = 00x.
$\overline{\text{CAS}}$	I/O/T	**SDRAM Column Access Strobe.** In conjunction with $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.

<table>
<tr><th>Mnemonic</th><th>Type</th><th>Function</th></tr>
<tr><td>CLK_CFG1–0</td><td>I</td><td>Core/CLKIN Ratio Control. SHARC Melody Ultra core clock (instruction cycle) rate is equal to n × PLLICLK where n is user selectable to 2, 3, or 4, using the CLK_CFG1–0 inputs. These pins can also be used in combination with the CLKDBL pin to generate additional core clock rates of 6 × CLKIN and 8 × CLKIN (see the Clock Rate Ratios table in the CLKDBL description).</td></tr>
<tr><td>CLKDBL</td><td>I</td><td>Crystal Double Mode Enable. This pin is used to enable the 2× clock double circuitry, where CLKOUT can be configured as either 1× or 2× the rate of CLKIN. This CLKIN double circuit is primarily intended to be used for an external crystal in conjunction with the internal clock generator and the XTAL pin. The internal clock generator, when used in conjunction with the XTAL pin and an external crystal, is designed to support up to a maximum of 25 MHz external crystal frequency. CLKDBL can be used in XTAL mode to generate a 50 MHz input into the PLL. The 2× clock mode is enabled (during RESET low) by tying CLKDBL to GND, otherwise it is connected to V_{DDEXT} for 1× clock mode. For example, this enables the use of a 25 MHz crystal to enable 100 MHz core clock rates and a 50 MHz CLKOUT operation when CLK_CFG1= 0, CLK_CFG1= 0, and CLKDBL = 0. This pin can also be used to generate different clock rate ratios for external clock oscillators. The possible clock rate ratio options (up to 100 MHz) for either CLKIN (external clock oscillator) or XTAL (crystal input) are as follows:

Clock Rate Ratios
<table>
<tr><th>CLKDBL</th><th>CLK_CFG1</th><th>CLK_CFG0</th><th>Core:CLKIN</th><th>CLKIN:CLKOUT</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>2:1</td><td>1×</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3:1</td><td>1×</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4:1</td><td>1×</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>4:1</td><td>2×</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>6:1</td><td>2×</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8:1</td><td>2×</td></tr>
</table>
An 8:1 ratio enables the use of a 12.5 MHz crystal to generate a 100 MHz core (instruction clock) rate and a 25 MHz CLKOUT (external port) clock rate. See Figure 13.
Note that when using an external crystal, the maximum crystal frequency cannot exceed 25 MHz. For all other external clock sources, the maximum CLKIN frequency is 50 MHz.</td></tr>
<tr><td>CLKIN</td><td>I</td><td>Local Clock In. Used in conjunction with XTAL. CLKIN is the SHARC Melody Ultra clock input. It configures the SHARC Melody Ultra to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the SHARC Melody Ultra to use the external clock source such as an external clock oscillator.The SHARC Melody Ultra external port cycles at the frequency of CLKIN. The instruction cycle rate is a multiple of the CLKIN frequency; it is programmable at power-up via the CLK_CFG1–0 pins. CLKIN may not be halted, changed, or operated below the specified frequency.</td></tr>
<tr><td>CLKOUT</td><td>O/T</td><td>Local Clock Out. CLKOUT is 1× or 2× and is driven at either 1× or 2× the frequency of CLKIN frequency by the current bus master. The frequency is determined by the CLKDBL pin. This output is three-stated when the SHARC Melody Ultra is not the bus master or when the host controls the bus (HBG asserted). A keeper latch on the DSP's CLKOUT pin maintains the output at the level to which it was last driven. This latch is only enabled on the SHARC Melody Ultra with ID2–0 = 00x.
If CLKDBL enabled, CLKOUT = 2 × CLKIN
If CLKDBL disabled, CLKOUT = 1 × CLKIN
Note that CLKOUT is controlled only by the CLKDBL pin and operates at either 1 × CLKIN or 2 × CLKIN.
Do not use CLKOUT in multiprocessing systems; use CLKIN instead.</td></tr>
<tr><td>CS</td><td>I/A</td><td>Chip Select. Asserted by host processor to select the SHARC Melody Ultra.</td></tr>
<tr><td>DATA47–16</td><td>I/O/T</td><td>External Bus Data. The SHARC Melody Ultra inputs and outputs data and instructions on these pins. Pull-up resistors on unused data pins are not necessary. A keeper latch on the DSP's DATA47–16 pins maintains the input at the level to which it was last driven. This latch is only enabled on the SHARC Melody Ultra with ID2–0 = 00x.

Note that DATA[15:8] pins (multiplexed with L1DATA[7:0]) can also be used to extend the data bus if the link ports are disabled and will not be used. In addition, DATA[7:0] pins (multiplexed with L0DATA[7:0]) can also be used to extend the data bus if the link ports are not used. This enables execution of 48-bit instructions from external SBSRAM (system clock speed-external port), SRAM (system clock speed-external port) and SDRAM (core clock or one-half the core clock speed). The IPACKx instruction packing mode bits in SYSCON should be set correctly (IPACK1–0 = 0x1) to enable this full instruction width/no-packing mode of operation.</td></tr>
</table>

Mnemonic	Type	Function
$\overline{\text{DMAG1}}$	O/T	**DMA Grant 1** (DMA Channel 11). Asserted by SHARC Melody Ultra to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{\text{DMAG1}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0 = 00x.
$\overline{\text{DMAG2}}$	O/T	**DMA Grant 2** (DMA Channel 12). Asserted by the SHARC Melody Ultra to indicate that the requested DMA starts on the next cycle. Driven by the bus master only. $\overline{\text{DMAG2}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0 = 00x.
$\overline{\text{DMAR1}}$	I/A	**DMA Request 1** (DMA Channel 11). Asserted by external port devices to request DMA services. $\overline{\text{DMAR1}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0 = 00x.
$\overline{\text{DMAR2}}$	I/A	**DMA Request 2** (DMA Channel 12). Asserted by external port devices to request DMA services. $\overline{\text{DMAR2}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0 = 00x.
DQM	O/T	**SDRAM Data Mask.** In write mode, DQM has a latency of zero and is used during a precharge command and during SDRAM power-up initialization.
DxA	I/O	**Data Transmit or Receive Channel A** (Serial Ports 0, 1, 2, 3). Each DxA pin has an internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
DxB	I/O	**Data Transmit or Receive Channel B** (Serial Ports 0, 1, 2, 3). Each DxB pin has an internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
EBOOT	I	**EPROM Boot Select**. For a description of how this pin operates, see Table 3 on page 18. This signal is a system configuration selection that should be hardwired.
$\overline{\text{EMU}}$	(O/D)	**Emulation Status**. Must be connected to the SHARC Melody Ultra Analog Devices' DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has an internal pull-up resistor.
FLAG11–0	I/O/A	**Flag Pins**. Each pin is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
FSx	I/O	**Transmit or Receive Frame Sync** (Serial Ports 0, 1, 2, 3). The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally. It can be active high or low or an early or late frame sync, in reference to the shifting of serial data.
GND	G	**Power Supply Return** (26 pins).
$\overline{\text{HBG}}$	I/O	**Host Bus Grant**. Acknowledges an $\overline{\text{HBR}}$ bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the SHARC Melody Ultra until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the SHARC Melody Ultra bus master and is monitored by all others. After $\overline{\text{HBR}}$ is asserted, and before $\overline{\text{HBG}}$ is given, $\overline{\text{HBG}}$ will float for 1 t_{CK} (1 CLKIN cycle). To avoid erroneous grants, $\overline{\text{HBG}}$ should be pulled up with a 20 kΩ to 50 kΩ external resistor.
$\overline{\text{HBR}}$	I/A	**Host Bus Request**. Must be asserted by a host processor to request control of the SHARC Melody Ultra processor's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the SHARC Melody Ultra that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the SHARC Melody Ultra places the address, data, select, and strobe lines in a high impedance state. $\overline{\text{HBR}}$ has priority over all SHARC Melody Ultra bus requests ($\overline{\text{BR}}$6–1) in a multiprocessing system.
ID2–0	I	**Multiprocessing ID.** Determines which multiprocessing bus request ($\overline{\text{BR}}$6–1) is used by the SHARC Melody Ultra. ID = 001 corresponds to $\overline{\text{BR1}}$, ID = 010 corresponds to $\overline{\text{BR2}}$, and so on. Use ID = 000 or ID = 001 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset.
$\overline{\text{IRQ}}$2–0	I/A	**Interrupt Request Lines.** These pins are sampled on the rising edge of CLKIN and may be either edge-triggered or level-sensitive.
LBOOT	I	**Link Boot.** For a description of how this pin operates, see Table 3 on page 18. This signal is a system configuration selection that should be hardwired.
LxACK	I/O	**Link Port Acknowledge** (Link Ports 0–1). Each LxACK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.
LxCLK	I/O	**Link Port Clock** (Link Ports 0–1). Each LxCLK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.

Mnemonic	Type	Function
LxDAT7–0 [DATA15–0]	I/O [I/O/T]	**Link Port Data** (Link Ports 0–1). For silicon revisions 1.2 and higher, each LxDAT pin has a keeper latch that is enabled when used as a data pin, or a 20 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. For silicon revisions 0.3, 1.0, and 1.1, each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. Note that L1DATA[7:0] are multiplexed with the DATA[15:8] pins; L0DATA[7:0] are multiplexed with the DATA[7:0] pins. If link ports are disabled and are not be used, these pins can be used as additional data lines for executing instructions at up to the full clock rate from external memory. See DATA47–16 for more information.
MISO	I/O (O/D)	**SPI Master In Slave Out.** If the SHARC Melody Ultra is configured as a master, the MISO pin becomes a data receive (input) pin. If the SHARC Melody Ultra is configured as a slave, the MISO pin becomes a data transmit (output) pin. In a SHARC Melody Ultra SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has an internal pull-up resistor. MISO can be configured as O/D by setting the OPD bit in the SPICTL register. Note that only one slave is enabled to transmit data at any given time.
MOSI	I/O (O/D)	**SPI Master Out Slave In.** If the SHARC Melody Ultra is configured as a master, the MOSI pin becomes a data transmit (output) pin. If the SHARC Melody Ultra is configured as a slave, the MOSI pin becomes a data receive (input) pin. In a SHARC Melody Ultra SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has an internal pull-up resistor.
$\overline{\text{MS}}$3–0	I/O/T	**Memory Select Lines.** These outputs are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank sizes are fixed to 16 Mwords for non-SDRAM and 64 Mwords for SDRAM. The $\overline{\text{MS}}$3–0 outputs are decoded memory address lines. In asynchronous access mode, the $\overline{\text{MS}}$3–0 outputs transition with the other address outputs. In synchronous access modes, the $\overline{\text{MS}}$3–0 outputs assert with the other address lines; however, they de-assert after the first CLKIN cycle in which ACK is sampled asserted. In a multiprocessor systems, the $\overline{\text{MS}}$x signals are tracked by slave SHARCs. The internal addresses 24 and 26 are zeros and 26 and 27 are decoded into $\overline{\text{MS}}$3–0.
NC		**Do Not Connect.** Reserved pins that must be left open and unconnected (5 pins).
$\overline{\text{PA}}$	I/O/T	**Priority Access.** Asserting its $\overline{\text{PA}}$ pin enables a SHARC Melody Ultra bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{PA}}$ is connected to all SHARC Melody Ultra processors in the system. If access priority is not required in a system, the $\overline{\text{PA}}$ pin should be left unconnected. $\overline{\text{PA}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0 = 00x.
$\overline{\text{RAS}}$	I/O/T	**SDRAM Row Access Strobe.** In conjunction with $\overline{\text{CAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, this pin defines the operation for the SDRAM to perform.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** $\overline{\text{RD}}$ is asserted whenever the SHARC Melody Ultra reads a word from external memory or from the IOP registers of other SHARC Melody Ultra processors. External devices, including other SHARC Melody Ultra processors, must assert $\overline{\text{RD}}$ for reading a word of the SHARC Melody Ultra IOP register memory. In a multiprocessing system, $\overline{\text{RD}}$ is driven by the bus master. $\overline{\text{RD}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0 = 00x.
REDY	O (O/D)	**Host Bus Acknowledge.** The SHARC Melody Ultra deasserts REDY (low) to add wait states to a host access of its IOP registers when $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the SHARC Melody Ultra to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
RPBA	I/S	**Rotating Priority Bus Arbitration Select**. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every SHARC Melody Ultra. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every SHARC Melody Ultra.
$\overline{\text{RSTOUT}}$	O	**Reset Out.** When $\overline{\text{RSTOUT}}$ is asserted (low), this pin indicates that the core blocks are in reset. It is deasserted 4096 cycles after $\overline{\text{RESET}}$ is deasserted indicating that the PLL is stable and locked. ($\overline{\text{RSTOUT}}$ exists only for silicon revision 1.2.)
$\overline{\text{SBTS}}$	I/S	**Suspend Bus and Three-State.** External devices can assert $\overline{\text{SBTS}}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the SHARC Melody Ultra attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/SHARC Melody Ultra deadlock.

Mnemonic	Type	Function
SCLKx	I/O	**Transmit/Receive Serial Clock** (Serial Ports 0, 1, 2, 3). Each SCLK pin has an internal pull-up resistor. This signal can be either internally or externally generated.
SDA10	O/T	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a non-SDRAM accesses or host accesses.
SDCLK0	I/O/S/T	**SDRAM Clock Output 0.** Clock for SDRAM devices.
SDCLK1	O/S/T	**SDRAM Clock Output 1.** Additional clock for SDRAM devices. For systems with multiple SDRAM devices, this pin handles the increased clock load requirements, eliminating the need for off-chip clock buffers. Either SDCLK1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	**SDRAM Clock Enable.** Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
$\overline{\text{SDWE}}$	I/O/T	**SDRAM Write Enable.** In conjunction with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, SDCLKx, and sometimes SDA10, this pin defines the operation for the SDRAM to perform.
SPICLK	I/O	**Serial Peripheral Interface Clock Signal.** Driven by the master, this signal controls the rate at which data is transferred. The master may transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock that is active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (high). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge of the clock and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has an internal pull-up resistor.
$\overline{\text{SPIDS}}$	I	**Serial Peripheral Interface Slave Device Select**. An active low signal used to enable slave devices. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode, $\overline{\text{SPIDS}}$ signal can be asserted to a master device to signal that an error has occurred because some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single-master, multiple-slave configuration where FLAG3–0 are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For SHARC Melody Ultra to SHARC Melody Ultra SPI interaction, any of the master SHARC Melody Ultra processors' FLAG3–0 pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the SHARC Melody Ultra SPI slave device.
TCK	I	**Test Clock** (JTAG). Provides a clock for JTAG boundary scan.
TDI	I/S	**Test Data Input** (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output** (JTAG). Serial scan output of the boundary scan path.
TIMEXP	O	**Timer Expired.** Asserted for four core clock cycles when the timer is enabled.
TMS	I/S	**Test Mode Select** (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
$\overline{\text{TRST}}$	I/A	**Test Reset** (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) After power-up or held low for proper operation of the SHARC Melody Ultra. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
V_{DDINT}	P	**Core Power Supply**. Nominally 1.8 V dc and supplies the DSP's core processor (14 pins).
V_{DDEXT}	P	**I/O Power Supply.** Nominally 3.3 V dc (13 pins).
$\overline{\text{WR}}$	I/O/T	**Memory Write Low Strobe.** $\overline{\text{WR}}$ is asserted when the SHARC Melody Ultra writes a word to external memory or the IOP registers of other SHARC Melody Ultra processors. External devices must assert $\overline{\text{WR}}$ for writing to the SHARC Melody Ultra's IOP registers. In a multiprocessing system, $\overline{\text{WR}}$ is driven by the bus master. $\overline{\text{WR}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0 = 00x.
XTAL	O	**Crystal Oscillator** Terminal 2. Used in conjunction with CLKIN to enable the SHARC Melody Ultra's internal clock oscillator or to disable it to use an external clock source. See CLKIN.

BOOT MODES

Table 3. Boot Mode Selection

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select).
0	0	1 (Input)	Host Processor.
0	1	0 (Input)	Serial Boot via SPI.
0	1	1 (Input)	Link Port.
0	0	0 (Input)	No Booting. Processor executes from external memory.
1	1	x (Input)	Reserved.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 4.

Parameter		Test Conditions	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage		1.71	1.89	1.71	1.89	V
AV_{DD}	Analog (PLL) Supply Voltage		1.71	1.89	1.71	1.89	V
V_{DDEXT}	External (I/O) Supply Voltage		3.13	3.47	3.13	3.47	V
V_{IH}	High Level Input Voltage[1]	@ V_{DDEXT} = max	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	V
V_{IL}	Low Level Input Voltage[1]	@ V_{DDEXT} = min	–0.5	0.8	–0.5	0.8	V
T_{CASE}	Case Operating Temperature[2]		–40	+105	0	+85	°C

[1]Applies to input and bidirectional pins: DATA47–16, ADDR23–0, $\overline{MS}$3–0, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, IRQ2–0, FLAG11–0, $\overline{HBG}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}$6–1, ID2–0, RPBA, $\overline{PA}$, $\overline{BRST}$, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCLK0, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{BMS}$, SDCKE, CLK_CFGx, $\overline{CLKDBL}$, CLKIN, $\overline{RESET}$, TRST, TCK, TMS, TDI.

[2]See the Thermal Characteristics section on page 24 for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Table 5.

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4]	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
I_{IHC}	CLKIN High Level Input Current[5]	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max		25	µA
I_{ILC}	CLKIN Low Level Input Current[5]	@ V_{DDEXT} = max, V_{IN} = 0 V		25	µA
I_{IKH}	Keeper High Load Current[6]	@ V_{DDEXT} = max, V_{IN} = 2.0 V	–250	–100	µA
I_{IKL}	Keeper Low Load Current[6]	@ V_{DDEXT} = max, V_{IN} = 0.8 V	50	200	µA
I_{IKH-OD}	Keeper High Overdrive Current[6, 7, 8]	@ V_{DDEXT} = max	–300		µA
I_{IKL-OD}	Keeper Low Overdrive Current[6, 7, 8]	@ V_{DDEXT} = max	300		µA
I_{ILPU}	Low Level Input Current Pull-Up[4]	@ V_{DDEXT} = max, V_{IN} = 0 V		250	µA
I_{OZH}	Three-State Leakage Current[9, 10, 11]	@ V_{DDEXT}= max, V_{IN} = V_{DDEXT} max		10	µA
I_{OZL}	Three-State Leakage Current[9, 12, 13]	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
I_{OZLPU1}	Three-State Leakage Current Pull-Up1[10]	@ V_{DDEXT} = max, V_{IN} = 0 V		500	µA
I_{OZLPU2}	Three-State Leakage Current Pull-Up2[11]	@ V_{DDEXT} = max, V_{IN} = 0 V		250	µA
I_{OZHPD1}	Three-State Leakage Current Pull-Down1[12]	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max		250	µA
I_{OZHPD2}	Three-State Leakage Current Pull-Down2[13]	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max		500	µA
$I_{DD-INPEAK}$	Supply Current (Internal)[14, 15]	t_{CCLK} = 10.0 ns, V_{DDINT} = max		900	mA
$I_{DD-INHIGH}$	Supply Current (Internal)[15, 16]	t_{CCLK} = 10.0 ns, V_{DDINT} = max		650	mA
$I_{DD-INLOW}$	Supply Current (Internal)[15, 17]	t_{CCLK} = 10.0 ns, V_{DDINT} = max		500	mA
$I_{DD-IDLE}$	Supply Current (Idle)[15, 18]	t_{CCLK} = 10.0 ns, V_{DDINT} = max		400	mA
AI_{DD}	Supply Current (Analog)[19]	@AV_{DD} = max		10	mA
C_{IN}	Input Capacitance[20, 21]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.8 V		4.7	pF

[1]Applies to output and bidirectional pins: DATA47–16, ADDR23–0, $\overline{MS}$3–0, $\overline{RD}$, $\overline{WR}$, ACK, DQM, FLAG11–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}$6–1, BMSTR, $\overline{PA}$, BRST, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDA10, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{BMS}$, SDCLKx, SDCKE, $\overline{EMU}$, XTAL, TDO, CLKOUT, TIMEXP, $\overline{RSTOUT}$.
[2]See the Output Drive Currents section on page 22 for typical drive current capabilities.
[3]Applies to input pins: DATA47–16, ADDR23–0, $\overline{MS}$3–0, $\overline{SBTS}$, IRQ2–0, FLAG11–0, $\overline{HBG}$, $\overline{HBR}$, $\overline{CS}$, $\overline{BR}$6–1, ID2–0, RPBA, BRST, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCLK0, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{BMS}$, SDCKE, CLK_CFGx, $\overline{CLKDBL}$, TCK, $\overline{RESET}$, CLKIN.
[4]Applies to input pins with 20 kΩ internal pull-ups: $\overline{RD}$, $\overline{WR}$, ACK, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{PA}$, TRST, TMS, TDI.
[5]Applies to CLKIN only.
[6]Applies to all pins with keeper latches: ADDR23–0, DATA47–0, $\overline{MS}$3–0, BRST, CLKOUT.
[7]Current required to switch from kept high to low or from kept low to high.
[8]Characterized, but not tested.
[9]Applies to three-statable pins: DATA47–16, ADDR23–0, $\overline{MS}$3–0, CLKOUT, FLAG11–0, REDY, $\overline{HBG}$, $\overline{BMS}$, $\overline{BR}$6-1, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, SDCLKx, SDCKE, SDA10, BRST.
[10]Applies to three-statable pins with 20 kΩ pull-ups: $\overline{RD}$, $\overline{WR}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{PA}$.
[11]Applies to three-statable pins with 50 kΩ internal pull-ups: DxA, DxB, SCLKx, SPICLK, $\overline{EMU}$, MISO, MOSI.
[12]Applies to three-statable pins with 50 kΩ internal pull-downs: LxDAT7–0 (below Revision1.2), LxCLK, LxACK. Use I_{OZHPD2} for Rev. 1.2 and higher.
[13]Applies to three-statable pins with 20 kΩ internal pull-downs: LxDAT7–0 (Revision 1.2 and higher).
[14]The test program used to measure $I_{DD-INPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see the Power Dissipation section on page 22.
[15]Current numbers are for V_{DDINT} and AV_{DD} supplies combined.
[16]$I_{DD-INHIGH}$ is a composite average based on a range of high activity code. See the Power Dissipation section on page 22.
[17]$I_{DD-INLOW}$ is a composite average based on a range of low activity code. See the Power Dissipation section on page 22.
[18]Idle denotes SHARC Melody Ultra state during execution of IDLE instruction. See the Power Dissipation section on page 22.
[19]Characterized, but not tested.
[20]Applies to all signal pins.
[21]Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +2.2 V
Analog (PLL) Supply Voltage (AV_{DD})	–0.3 V to +2.2 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING SPECIFICATIONS

The SHARC Melody Ultra processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL). This PLL based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock (the clock source for the external port logic and I/O pads).

The SHARC Melody Ultra processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, link ports, serial ports, and external port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 and $\overline{\text{CLKDBL}}$ pins. Even though the internal clock is the clock source for the external port, it behaves as described on the Clock Rate Ratio chart in the $\overline{\text{CLKDBL}}$ pin description in Table 2. To determine switching frequencies for the serial and link ports, divide down the internal clock using the programmable divider control of each port (DIVx for the serial ports and LxCLKD for the link ports).

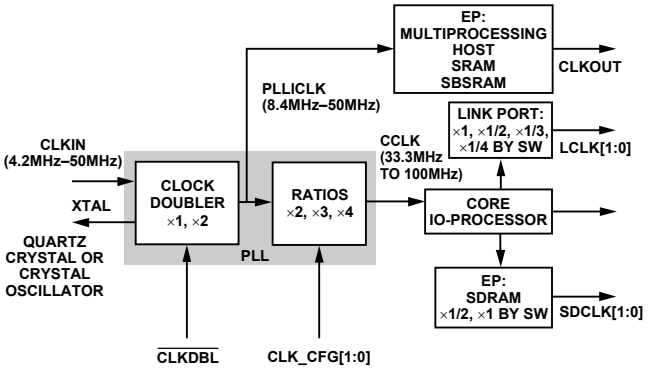

Figure 13. Core Clock and System Relationship to CLKIN

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation depends on the instruction execution sequence and the data operands involved. Using the current specifications ($I_{DD\text{-}INPEAK}$, $I_{DD\text{-}INHIGH}$, $I_{DD\text{-}INLOW}$, $I_{DD\text{-}IDLE}$) from the Electrical Characteristics (Table 5 on page 20), the programmer can estimate the SHARC Melody Ultra processor's internal power supply (V_{DDINT}) input current for a specific application, according to the following formula:

$$I_{DDINT} = \%\ Peak \times I_{DD\text{-}INPEAK} + \%\ High \times I_{DD\text{-}INHIGH} + \%\ Low \times I_{DD\text{-}INLOW} + \%\ Idle \times I_{DD\text{-}IDLE}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on

- The number of output pins that switch during each cycle (O)
- The maximum frequency at which they can switch (f)
- Their load capacitance (C)
- Their voltage swing (V_{DD})

and is calculated by

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/t_{CK}$ while writing to an SDRAM memory.

Example:

Estimate P_{EXT} with the following assumptions:

- A system with one bank of external memory (32 bit)
- Two 1M × 16 SDRAM chips are used, each with a load of 10 pF (ignoring trace capacitance)
- External data memory writes can occur every cycle at a rate of $1/t_{CK}$, with 50% of the pins switching
- The bus cycle time is 50 MHz
- The external SDRAM clock rate is 100 MHz
- SDRAM refresh cycles are ignored
- Addresses are incremental and on the same page

The P_{EXT} equation is calculated for each class of pins that can drive.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + P_{INT} + P_{PLL}$$

where P_{PLL} is $AI_{DD} \times 1.8$ V, using the value for AI_{DD} listed in the Electrical Characteristics (Table 5 on page 20).

OUTPUT DRIVE CURRENTS

Figure 14 shows typical I-V characteristics for the output drivers of the SHARC Melody Ultra. The curves represent the current drive capability of the output drivers as a function of output voltage.

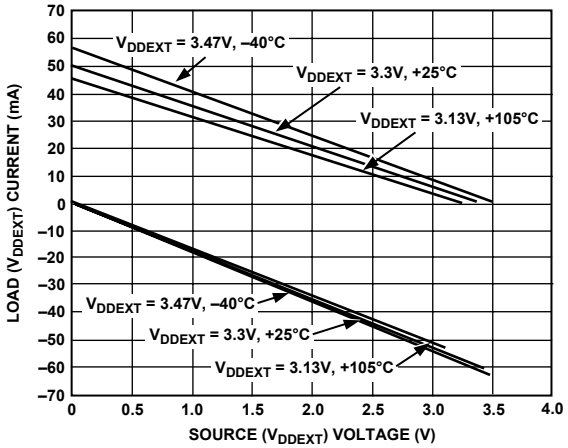

Figure 14. Typical Drive Currents

TEST CONDITIONS

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time, t_{ENA}, is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output has reached a specified high or low trip point, as shown in Figure 15. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the equation

$$t_{DECAY} = \frac{C_L \Delta V}{I_L}$$

The output disable time, t_{DIS}, is the difference between $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 15. The time $t_{MEASURED}$ is the

interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given previously. Choose ΔV to be the difference between the SHARC Melody Ultra processor's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line) and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time.

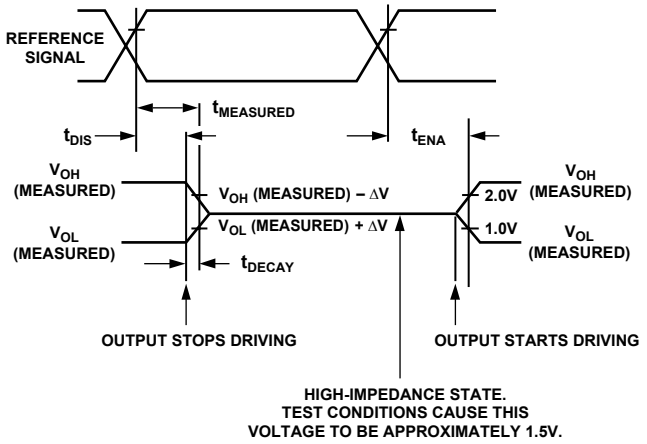

Figure 15. Output Enable/Disable

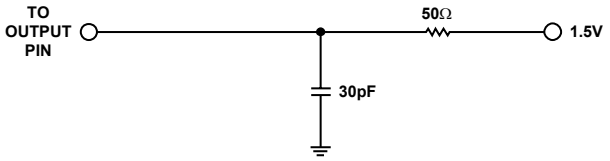

Figure 16. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

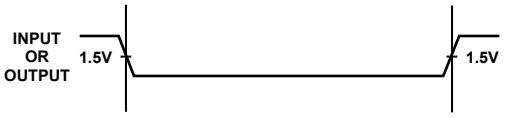

Figure 17. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 16). Figure 18 shows how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the Output Disable Time section.) The graphs of Figure 18, Figure 19, and Figure 20 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise/Fall Time (20%–80%, V = Min) vs. Load Capacitance.

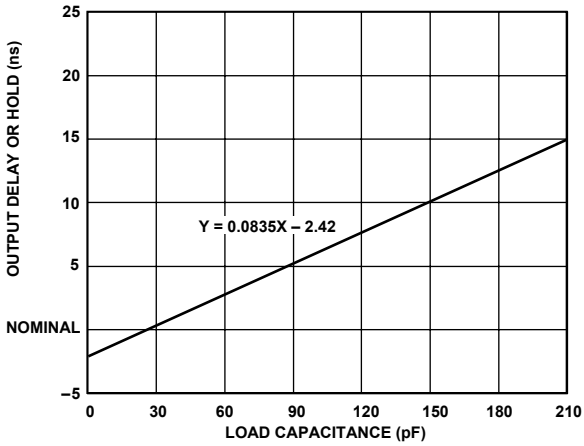

Figure 18. Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

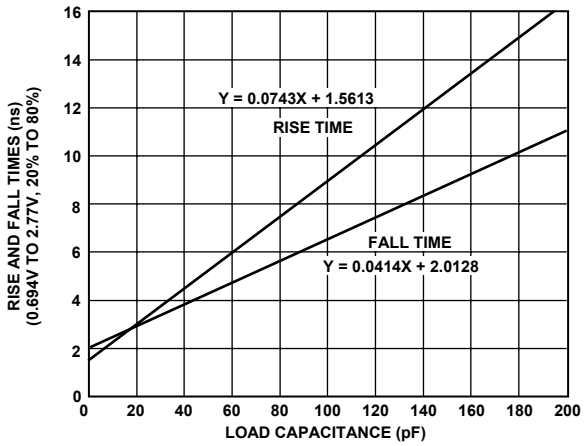

Figure 19. Typical Output Rise/Fall Time (20%–80%, V_{DDEXT} = Max)

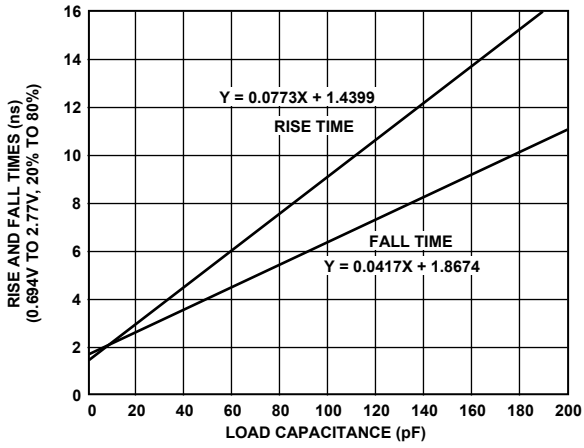

Figure 20. Typical Output Rise/Fall Time (20%–80%, V_{DDEXT} = Min)

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The SHARC Melody Ultra is packaged in a 225-lead Mini Ball Grid Array (MBGA). The SHARC Melody Ultra is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} specification is not exceeded, a heat sink and/or an airflow source may be used. Use the center block of ground pins (MBGA balls: F6–10, G6–10, H6–10, J6–10, K6–10) to provide thermal pathways to the printed circuit board's ground plane. A heat sink should be attached to the ground plane with a thermal adhesive as close as possible to the thermal pathways.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

where:

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown in the Power Dissipation section on page 22).

θ_{CA} = Value from Table 7, below.

Table 7. Airflow over Package vs. θ_{CA}

Airflow (Linear ft/min)	0	200	400
θ_{CA} (°C/W)[1]	17.9	15.2	13.7

[1] θ_{JC} = 6.8°C/W.

PIN CONFIGURATION

Table 8. 225-Lead Metric MBGA Pin Assignments

PBGA Pin Number	Mnemonic	PBGA Pin Number	Mnemonic	PBGA Pin Number	Mnemonic	PBGA Pin Number	Mnemonic	PBGA Pin Number	Mnemonic
A01	NC	D01	TDO	G01	FLAG1	K01	TIMEXP	N01	ADDR[14]
A02	BMSTR	D02	TCK	G02	FLAG2	K02	ADDR[22]	N02	ADDR[15]
A03	$\overline{\text{BMS}}$	D03	FLAG11	G03	FLAG4	K03	ADDR[20]	N03	ADDR[10]
A04	$\overline{\text{SPIDS}}$	D04	MISO	G04	FLAG3	K04	ADDR[23]	N04	ADDR[5]
A05	EBOOT	D05	SCLK0	G05	V_{DDEXT}	K05	V_{DDINT}	N05	ADDR[1]
A06	LBOOT	D06	D1B	G06	GND	K06	GND	N06	$\overline{\text{MS0}}$
A07	SCLK2	D07	FS1	G07	GND	K07	GND	N07	$\overline{\text{BR5}}$
A08	D3B	D08	V_{DDINT}	G08	GND	K08	GND	N08	$\overline{\text{BR2}}$
A09	L0DAT[4]	D09	SCLK3	G09	GND	K09	GND	N09	BRST
A10	L0ACK	D10	L0DAT[5]	G10	GND	K10	GND	N10	SDCKE
A11	L0DAT[2]	D11	L0DAT[3]	G11	V_{DDEXT}	K11	V_{DDINT}	N11	$\overline{\text{CS}}$
A12	L1DAT[6]	D12	L1DAT[5]	G12	DATA[34]	K12	DATA[22]	N12	CLK_CFG1
A13	L1CLK	D13	DATA[42]	G13	DATA[35]	K13	DATA[19]	N13	CLK_CFG0
A14	L1DAT[2]	D14	DATA[46]	G14	DATA[33]	K14	DATA[21]	N14	AV_{DD}
A15	NC	D15	DATA[44]	G15	DATA[32]	K15	DATA[23]	N15	$\overline{\text{DMAR1}}$
B01	$\overline{\text{TRST}}$	E01	FLAG10	H01	FLAG0	L01	ADDR[19]	P01	ADDR[13]
B02	TDI	E02	$\overline{\text{RESET}}$	H02	$\overline{\text{IRQ0}}$	L02	ADDR[17]	P02	ADDR[9]
B03	RPBA	E03	FLAG8	H03	V_{DDINT}	L03	ADDR[21]	P03	ADDR[8]
B04	MOSI	E04	D0A	H04	$\overline{\text{IRQ1}}$	L04	ADDR[2]	P04	ADDR[4]
B05	FS0	E05	V_{DDEXT}	H05	V_{DDINT}	L05	V_{DDEXT}	P05	$\overline{\text{MS2}}$
B06	SCLK1	E06	V_{DDINT}	H06	GND	L06	V_{DDINT}	P06	$\overline{\text{SBTS}}$
B07	D2B	E07	V_{DDEXT}	H07	GND	L07	V_{DDEXT}	P07	$\overline{\text{BR4}}$
B08	D3A	E08	V_{DDINT}	H08	GND	L08	V_{DDINT}	P08	$\overline{\text{BR1}}$
B09	L0DAT[7]	E09	V_{DDEXT}	H09	GND	L09	V_{DDEXT}	P09	SDCLK1
B10	L0CLK	E10	V_{DDINT}	H10	GND	L10	V_{DDINT}	P10	SDCLK0
B11	L0DAT[1]	E11	V_{DDEXT}	H11	V_{DDINT}	L11	V_{DDEXT}	P11	REDY
B12	L1DAT[4]	E12	L0DAT[0]	H12	DATA[29]	L12	$\overline{\text{CAS}}$	P12	CLKIN
B13	L1ACK	E13	DATA[39]	H13	DATA[28]	L13	DATA[20]	P13	DQM
B14	L1DAT[0]	E14	DATA[43]	H14	DATA[30]	L14	DATA[16]	P14	AGND
B15	$\overline{\text{RSTOUT}}$[1]	E15	DATA[41]	H15	DATA[31]	L15	DATA[18]	P15	$\overline{\text{DMAR2}}$
C01	TMS	F01	FLAG5	J01	$\overline{\text{IRQ2}}$	M01	ADDR[16]	R01	NC
C02	$\overline{\text{EMU}}$	F02	FLAG7	J02	ID1	M02	ADDR[12]	R02	ADDR[11]
C03	GND	F03	FLAG9	J03	ID2	M03	ADDR[18]	R03	ADDR[7]
C04	SPICLK	F04	FLAG6	J04	ID0	M04	ADDR[6]	R04	ADDR[3]
C05	D0B	F05	V_{DDINT}	J05	V_{DDEXT}	M05	ADDR[0]	R05	$\overline{\text{MS3}}$
C06	D1A	F06	GND	J06	GND	M06	$\overline{\text{MS1}}$	R06	$\overline{\text{PA}}$
C07	D2A	F07	GND	J07	GND	M07	$\overline{\text{BR6}}$	R07	$\overline{\text{BR3}}$
C08	FS2	F08	GND	J08	GND	M08	V_{DDEXT}	R08	$\overline{\text{RD}}$
C09	FS3	F09	GND	J09	GND	M09	$\overline{\text{WR}}$	R09	CLKOUT
C10	L0DAT[6]	F10	GND	J10	GND	M10	SDA10	R10	$\overline{\text{HBR}}$
C11	L1DAT[7]	F11	V_{DDINT}	J11	V_{DDEXT}	M11	$\overline{\text{RAS}}$	R11	$\overline{\text{HBG}}$
C12	L1DAT[3]	F12	DATA[37]	J12	DATA[26]	M12	ACK	R12	$\overline{\text{CLKDBL}}$
C13	L1DAT[1]	F13	DATA[40]	J13	DATA[24]	M13	DATA[17]	R13	XTAL
C14	DATA[45]	F14	DATA[38]	J14	DATA[25]	M14	$\overline{\text{DMAG1}}$	R14	$\overline{\text{SDWE}}$
C15	DATA[47]	F15	DATA[36]	J15	DATA[27]	M15	$\overline{\text{DMAG2}}$	R15	NC

[1]$\overline{\text{RSTOUT}}$ exists only for silicon revisions 1.2 and greater. Leave this pin unconnected for silicon revisions 0.3, 1.0, and 1.1.

PIN LAYOUT SUMMARY

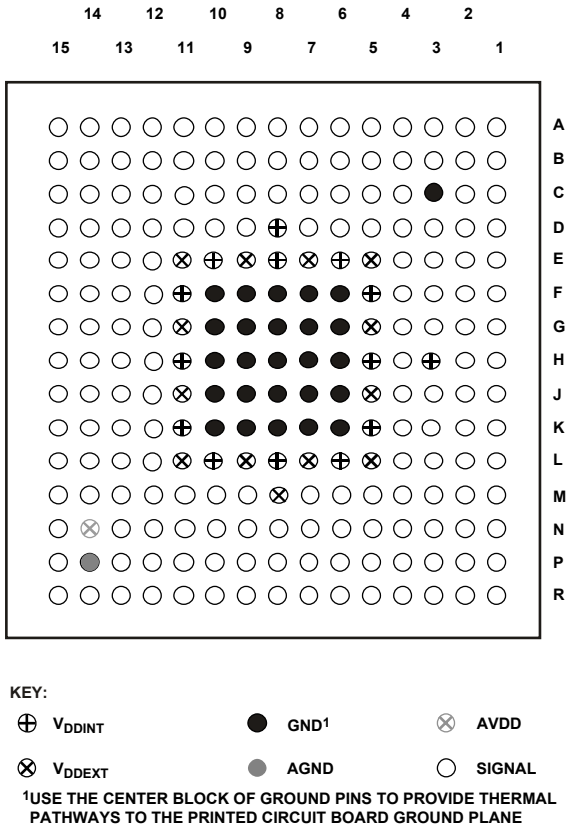

Figure 21. 225-Lead Metric MBGA Pin Assignments, Bottom View, Summary

OUTLINE DIMENSIONS

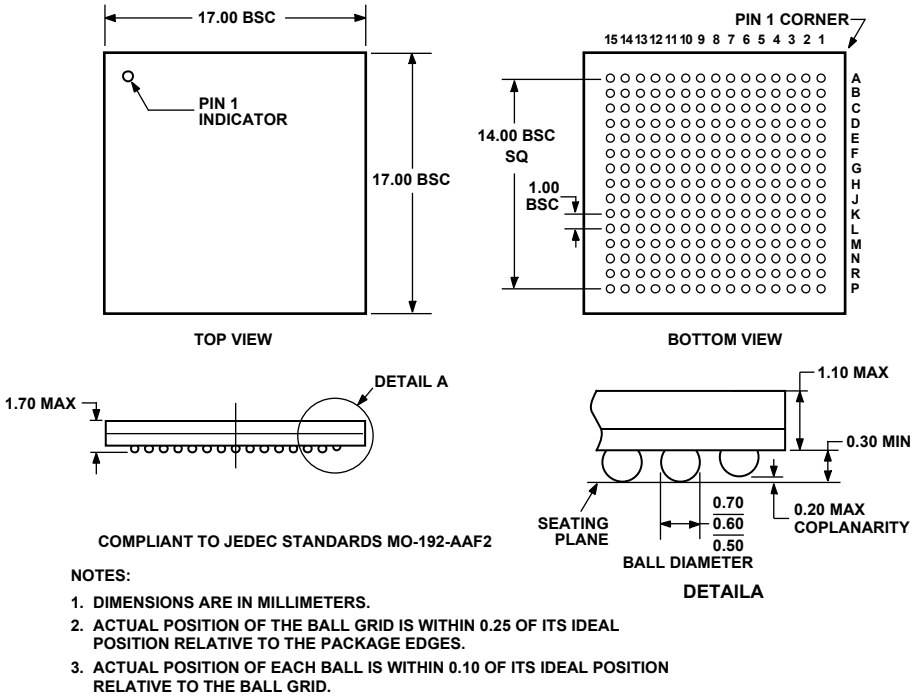

Figure 22. 225-Ball Mini-Ball Grid Array [MBGA]
(CA-225)
Dimensions shown in millimeters

ESD Caution

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Table 9.

Part Number[1, 2]	Case Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage
ADSST-21161NKCA100	0°C to +85°C	100 MHz	1 Mbit	1.8 V INT/3.3 V EXT
ADSST-21161NCCA100	–40°C to +105°C	100 MHz	1 Mbit	1.8 V INT/3.3 V EXT

[1]These parts are packaged in a 225-lead Mini-Ball Grid Array (MBGA).
[2]These products are sold as part of a chipset, bundled with necessary application software under special part numbers. Contact ADI directly for more information.

NOTES

C03373–0–10/03(0)